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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/800,630	03/16/2004	Kazuhiro Tashiro	042236	9692

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EXAMINER	
TRAN, MAI HUONG C	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/800,630	TASHIRO ET AL.	
	Examiner	Art Unit	
	Mai-Huong Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *1-4,21 and 22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/16/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

Application's election without traverse of Group I (Claims 5-20), species 1, drawn to a semiconductor device protection cover is acknowledged for prosecution in the subject application. Accordingly, claims 1-4 and 21-22 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Applicants have the right to file a divisional application covering the subject matter of the non-elected claims.

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 5-20 are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 6,057,597 to Farnworth et al.

Regarding to claim 5, Farnworth discloses a semiconductor device protection cover attached to a semiconductor device, comprising a base portion 14B; a first surface, said first surface 20B being flat; and a second surface 30 having a projecting portion to be brought into contact with a substrate 14B of the semiconductor device and a depressed portion not to be brought into contact with parts mounted in the semiconductor device (col. 3, lines 30-67, cols. 4-7, and fig. 7).

Regarding to claim 6, the semiconductor device protection cover wherein the semiconductor device protection cover has a structure able to be detachably attached to the semiconductor device (col. 3, lines 63-67).

Regarding to claim 9, the semiconductor device protection cover wherein the projecting portion and the base portion of the semiconductor device protection cover are formed from elastic materials (col. 4, lines 2-6).

Regarding to claim 10, the semiconductor device protection cover wherein the projecting portion and the base portion of the semiconductor device protection cover have conductivity (col. 5, line 24, figs. 4-6).

Regarding to claim 11, the semiconductor device protection cover further comprising an engaging portion that engages the semiconductor device protection cover

with the semiconductor device with the semiconductor device protection cover being attached to the semiconductor device (col. 4, lines 65-67, col. 5, lines 1-35).

Regarding to claim 12, the semiconductor device protection cover wherein the base portion has a predetermined shape irrespective of an outer shape of the semiconductor device (fig. 7).

Regarding to claim 13, a semiconductor device protection cover attached to a semiconductor device, comprising a base portion 30; a first surface 20B, said first surface being flat; and a second surface 30 to be brought into contact with a substrate of and parts mounted in the semiconductor device, said second surface being formed from an elastic material (cols. 3-4, and fig. 7).

Regarding to claim 14, a semiconductor device unit, comprising a semiconductor device; and a semiconductor device protection cover, wherein the semiconductor device protection cover comprises: a base portion; a first surface, said first surface being flat; and a second surface having a projecting portion to be brought into contact with a substrate of the semiconductor device and a depressed portion not to be brought into contact with parts mounted in the semiconductor device (cols. 3-4, and fig. 7).

Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7 and 8 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,057,597 to Farnworth et al. in view of the remark.

Regarding to claim 7, Farnworth discloses the semiconductor device protection cover, wherein the projecting portion and the base portion of the semiconductor device protection cover are formed from materials selected from the group consisting of plastic and metal but does not disclose the materials having hardness higher than a surface of the semiconductor device.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the projecting portion and the base portion of the semiconductor device protection cover with materials having hardness higher than a surface of the semiconductor device.

Regarding to claim 8, Farnworth discloses the semiconductor device protection cover, wherein the projecting portion and the base portion of the semiconductor device protection cover are formed from materials selected from the group consisting of plastic and metal but does not disclose the materials having hardness lower than a surface of the semiconductor device.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the projecting portion and the base portion of the semiconductor device protection cover with materials having hardness lower than a surface of the semiconductor device.

Claims 15- 20 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,057,597 to Farnworth et al. in view of US Patent No. 6,784,542 to Fukasawa et al.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or

(3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Regarding to claim 15, Farnworth discloses the claimed invention except for the semiconductor device unit, wherein the semiconductor device has a first positioning member; and the semiconductor device protection cover has a second positioning member, the semiconductor device and the semiconductor device protection cover being set in position when the first positioning member and the second positioning member are engaged with each other.

Fukasawa teaches the semiconductor device has a first positioning member; and the semiconductor device protection cover has a second positioning member, the semiconductor device and the semiconductor device protection cover being set in position when the first positioning member and the second positioning member are engaged with each other (figs. 19A-19C, 20A-20C).

. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the semiconductor device has a first positioning member; and the semiconductor device protection cover has a second positioning member, the

semiconductor device and the semiconductor device protection cover being set in position when the first positioning member and the second positioning member are engaged with each other, as taught by Fukasawa et al. in order to achieve such a real chip-size package structure, as well as for improving the efficiency of production of the semiconductor devices having such a package structure (col. 1, lines 26-28).

Regarding to claim 16, Fukasawa discloses the semiconductor device unit, wherein the first positioning member is a projection; and the second positioning member is a recess engagable with the projection (figs. 19A-19C, 20A-20C).

Regarding to claim 17, the semiconductor device unit, wherein an inclined surface is formed on the projection for guiding insertion of the projection into the recess (figs. 19A-19C).

Regarding to claim 18, the semiconductor device unit, wherein the first positioning member is a peripheral part of the semiconductor device; and the second positioning member is a wall engagable with the peripheral part (figs. 19A-19C).

Regarding to claim 19, the semiconductor device unit, wherein an inclined surface is formed on the second positioning member for guiding the first positioning member to engage with the second positioning member (figs. 19A-19C).

Regarding to claim 20, the semiconductor device unit, wherein the first positioning member and the second positioning member are formed by recognition marks (figs. 19A-19C).

Conclusion

Any inquiry concerning this communication on earlier communications from the examiner should be directed to Mai-Huong Tran, (571) 272-1796. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 6:30 PM. The examiner's supervisor, David Nelms can be reached on (571) 272-1787.

.The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mai-Huong Tran